and outputs a delay adjustment signal based on the first and second data signals; a first delay adjustment circuit which receives an output of the first register circuit and outputs a first delay adjusted data signal, a delay time of the first delay adjustment circuit being adjusted based on the delay adjustment signal; a second delay adjustment circuit which receives an output of the second register circuit and outputs a second delay adjusted data signal, a delay time of the second delay adjustment circuit being adjusted based on the delay adjustment signal; a first driver circuit which receives the first delay adjusted data signal; and a second driver circuit which receives the second delay adjusted data signal, wherein value of the delay adjustment signal changes in accordance with data pattern of the first and second data signals.--

IN THE ABSTRACT:

Please replace the Abstract as follows:

--A semiconductor integrated circuit device includes register circuits which receive data signals, a delay adjustment signal output circuit which receives the data signals and outputs delay adjustment signals based on the data signals, delay adjustment circuits which receive outputs of the register circuits and output delay adjusted data signals, and the driver circuits which receive the delay adjusted data signals. An output timing of each of the register circuits is controlled by a clock signal. A delay time of each of the delay adjustment circuits is adjusted based on the delay adjustment signals. Values of the delay adjustment signals change in accordance with data pattern of the data signals. --